REMARKS

Claims 1-57 are pending. Claim 38 is amended. In view of the following, all of the claims are in condition for allowance. If, after considering this response, the Examiner does not agree that all of the claims are allowable, she is requested to schedule a teleconference with the Applicant's attorney to further the prosecution of the application.

Rejection of claims 1-5, 10, 13-18, 22-25, 29, 31-35, 38-46, 51 and 53-56 under §103(a) as being unpatentable over Sacks et al. (US 6,181,505) in view of Tuttle et al. (US 6,108,151)

Claim 1

Claim 1 recites a servo circuit, comprising a processor operable to detect a servo wedge while a disk is attaining or after the disk attains an operating speed but before a servo channel recovers any servo data.

For example, referring, *e.g.*, to FIGS. 4 and 6 and paragraphs 30, 39, 41-60 and 62 of the present application, a servo wedge 22 includes a preamble 74, a servo synchronization mark (SSM) 76, head-location identifier 78 and bursts 84a-84n. On disk spin up, a processor 40 of a servo circuit 30 exploits the properties of a sinusoid to detect the preamble 74, and thus detect the servo wedge 22, before a servo channel 34 actually recovers any servo data. After the processor 40 detects the servo wedge 22, it searches for the SSM 76 within a predetermined time window, and then recovers the location identifier 78, which a head-position circuit 214 uses to determine an initial position of a read-write head 32. This technique allows the processor 40 to detect a servo wedge on disk spin up without the need for the disk to include spin-up wedges, which are often relatively long fields of consecutive logic 0's. By eliminating spin-up wedges, one can increase the disk's data-storage capacity.

In contrast, Sacks must recover servo data before detecting a servo wedge. The Examiner concedes on page 2 of the Office Action that "Sacks et al. fails to teach a processor operable to detect one of the servo wedges during or after disk spin-up search operation without first detecting a spin-up wedge." To detect a spin-up wedge, which comprises servo data, Sacks must first recover (*i.e.*, read) this data to determine whether or not the data composes a spin-up wedge. But as discussed above, the claimed servo circuit can detect a servo wedge before recovering servo data.

Similarly, Tuttle et al. '151, like Sacks, must recover servo data before detecting a servo wedge. Referring, *e.g.*, to Tuttle's FIG. 3 and col. 15, lines 13-30, a servo address mark (*i.e.*, spin-up wedge) detector A126 must recover, *i.e.*, read, a servo address mark, which is typically a "long sequence of '0' bits," before the detector A126 detects a servo wedge.

Therefore, neither Sacks, Tuttle, nor the combination of Sacks and Tuttle suggests detecting a servo wedge while a disk is attaining or after the disk attains an operating speed but before recovering any servo data.

Claim 22

Claims 22 is patentable for reasons similar to those recited above in support of the patentability of claim 1.

Claim 38

Claim 38, as amended, recites a method, comprising detecting servo data that identifies application data stored on the data-storage disk before recovering any servo data in the form of a logic level.

For example, referring, *e.g.*, to FIGS. 7, 11 and 12 and the corresponding disclosure in the present application, the processor 40 exploits the properties of a sinusoid to detect the preamble 74, and thus detect the servo wedge 22, before a servo

channel 34 actually recovers any servo data in the form of a logic level. It should be noted that "detecting" servo data and "recovering" servo data are entirely different operations. The preamble 74 (and thus servo wedge 22) is detected by exploiting the properties of a sinusoid without actually recovering any servo data in the form of logic 0's or 1's. Amplitude samples 140, 142 of the preamble sinusoid are taken and used to calculate a peak amplitude Y to determine detection of the preamble 74. Because the amplitude samples 140, 142 represent analog values, no actual servo data (logic 0's or 1's) is recovered. As a result, the processor 40 is able to detect the preamble 74 (and thus servo wedge 22) before recovering any actual servo data in the form of a logic level (l0's or 1's).

In contrast, Sacks must recover servo data in the form of a logic level (0's or 1's) before detecting a servo wedge. The Examiner concedes on page 2 of the Office Action that "Sacks et al. fails to teach a processor operable to detect one of the servo wedges during or after disk spin-up search operation without first detecting a spin-up wedge." To detect a spin-up wedge, which comprises servo data in the form of a logic level (0's or 1's), Sacks must first recover this data to determine whether or not the data composes a spin-up wedge. But as discussed above, the claimed servo circuit can detect a servo wedge before recovering any servo data in the form of a logic level.

Similarly, Tuttle et al. '151, like Sacks, must recover servo data in the form of a logic level (0's or 1's) before detecting a servo wedge. Referring, *e.g.*, to col. 15, lines 13-30 of Tuttle, a servo address mark (*i.e.,* spin-up wedge) detector A126 must recover a servo address mark (special sequence of logic bits), which is typically a "long sequence of '0' bits," before the detector A126 detects a servo wedge. In other words, Tuttle must recover a long sequence of servo data in the form of a logic level (logic 0's) before it is able to detect any servo wedge.

Therefore, neither Sacks, Tuttle, nor the combination of Sacks and Tuttle suggests detecting servo data that identifies application data stored on the data-storage disk before recovering any servo data in the form of a logic level.

Claims 2-18, 23-35 and 39-56

Claims 2-18, 23-35 and 39-57 are patentable by virtue of their respective dependencies from independent claims 1, 22 and 38.

Rejection of claims 19, 36 and 57 under §103(a) as being unpatentable over Sacks et al. and Tuttle et al., and further in view of Patapoutian et al. (US 5,661,760)

Claims 19, 36 and 57 are patentable by virtue of their respective dependencies from independent claims 1, 22 and 38.

Rejection of claims 20 and 37 under §103(a) as being unpatentable over Sacks et al. and Tuttle et al., and further in view of Patapoutian et al. and Cloke et al. (US 5,822,143)

Claims 20 and 37 are patentable by virtue of their respective dependencies from independent claims 1 and 22.

Rejection of claim 21 under §103(a) as being unpatentable over Sacks et al. and Tuttle et al., and further in view of Ehrlich et al. (US 6,519,107)

Claim 21 is patentable by virtue of its dependency from independent claim 1.

CONCLUSION

In light of the foregoing, claims 1-57 are in condition for allowance, which is respectfully requested.

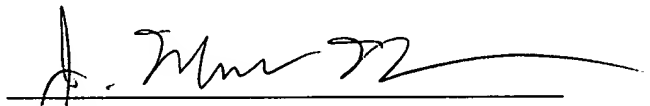
In the event any fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner schedule a phone interview with the Applicants' attorney, J. Mark Han or Bryan Santarelli, at (425) 455-5575.

DATED this 20th day of December, 2005.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP



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